IN THE CLAIMS

Please cancel claims 1-31 and add new claims 32-61 as set forth below:

1-31 (cancelled).

32 (new). A memory cell comprising:

an access device; and

a memory element operatively coupled to the access device, the memory element comprising:

a dielectric material having a container formed therein;

a first electrode disposed within the container, the first electrode having a tip comprising carbon;

a memory material disposed over the tip of the first electrode; and

a second electrode disposed over to the memory material.

33 (new). The memory cell, as set forth in claim 32, wherein the access device comprises a diode.

34 (new). The memory cell, as set forth in claim 32, wherein a portion of the container that bounds the first electrode is smaller than the photolithographic limit.

35 (new). The memory cell, as set forth in claim 32, wherein the first electrode comprises a conductive material having a layer of carbon thereon to form the tip.

36 (new). The memory cell, as set forth in claim 32, wherein the memory material comprises structure changing material.

37 (new). The memory cell, as set forth in claim 36, wherein the structure changing material comprises a material which changes between different states of crystallinity in response to electrical stimulus.

38 (new). The memory cell, as set forth in claim 37, wherein each of the different states of crystallinity corresponds to a given resistance level.

39 (new). The memory cell, as set forth in claim 32, wherein the memory material comprises a chalcogenide material.

40 (new). The memory cell, as set forth in claim 32, wherein the memory material comprises a programmable resistive element.

41 (new). The memory cell, as set forth in claim 40, wherein the programmable resistive element changes between different resistance levels in response to electrical stimulus.

42 (new). The memory cell, as set forth in claim 32, wherein the access device and the memory element are disposed wholly in an area defined by an intersection of a word line and a bit line.

43 (new). The memory cell, as set forth in claim 32, wherein the memory material comprises solid, amorphous chalcogenide containing selenium.

44 (new). The memory cell, as set forth in claim 32, wherein the access device controls electrical current through the memory element.

45 (new). The memory cell, as set forth in claim 32, wherein the access device is disposed in line with the memory element.

46 (new). The memory cell, as set forth in claim 32, wherein the access device and the memory element have substantially the same cross-sectional area.

47 (new). The memory cell, as set forth in claim 32, wherein the memory element and the access device comprise substantially the same lateral areas and wherein the memory element is disposed directly over the access device.

48 (new). A memory cell comprising:

a memory element comprising a memory material disposed between a first electrode and a second electrode, the first electrode being disposed within a pore formed in a dielectric material; and

an access device being coupled to the first electrode and being self-aligned with the memory element.

49 (new). The memory cell, as set forth in claim 48, wherein the access device comprises a diode.

50 (new). The memory cell, as set forth in claim 49, wherein the diode comprises N doped polysilicon disposed adjacent P doped polysilicon.

51 (new). The memory cell, as set forth in claim 48, wherein the memory material comprises structure changing material.

52 (new). The memory cell, as set forth in claim 51, wherein the structure changing material comprises a material which changes between different states of crystallinity in response to electrical stimulus.

53 (new). The memory cell, as set forth in claim 52, wherein each of the different states of crystallinity corresponds to a given resistance level.

54 (new). The memory cell, as set forth in claim 48, wherein the memory material comprises a chalcogenide material.

55 (new). The memory cell, as set forth in claim 48, wherein the memory material comprises a programmable resistive element.

56 (new). The memory cell, as set forth in claim 55, wherein the programmable resistive element changes between different resistance levels in response to electrical stimulus.

57 (new). The memory cell, as set forth in claim 48, wherein the memory material comprises solid, amorphous chalcogenide containing selenium.

58 (new). The memory cell, as set forth in claim 48, wherein the access device controls electrical current through the memory element.

59 (new). The memory cell, as set forth in claim 48, wherein the access device is disposed in line with the memory element.

60 (new). The memory cell, as set forth in claim 48, wherein the access device and the memory element have substantially the same cross-sectional area.

61 (new). The memory cell, as set forth in claim 48, wherein the memory element and the access device comprise substantially the same lateral areas and wherein the memory element is disposed directly over the access device.